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| 09/608,624 | 06/30/2000 | Stephen Jourdan | 2207/8609 | 9451 |

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| TSAI, HENRY | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2183 | |

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Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/608,624 | JOURDAN ET AL. | |
| | Examiner | Art Unit | |
| | Henry W.H. Tsai | 2183 | |

*-- The MAILING DATE of this communication appears on th cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *04 October 2004* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-7,9-20,22-30 and 38-43* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *4-7,9-15 and 23-27* is/are allowed.

6)☒ Claim(s) *1-3,16,20,22,28-30 and 38-43* is/are rejected.

7)☒ Claim(s) *17-19* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. §§ 119 and 120**

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *11/16/04* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

**DETAILED ACTION**

***Claim Objections***

1. Claims 38-40 are objected to because of the following informalities: in claim 38, line 3, it is not clear which memory is referred to as "the memory entry" since there may have many memory entries. It is suggested to change "the memory entry" to -the at least one memory entry".

Appropriate correction is required.

***Claim Rejections - 35 USC § 112***

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 3, 22, 30 and 40-43 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 41, it is not clear why it requires means for indexing the only one trace by an address of a last instruction. Means for indexing the trace by an address of a last instruction is redundant since only one trace exists in the claimed memory entry. Similar problems exist in claims 3, 22, 30, 40 and 43.

In claim 42, it is not clear why it requires means for indexing the trace when there is only one memory entry storing one trace. Means for indexing the trace by an address of a last instruction is redundant when only one trace exists in only one claimed memory entry.

Applicant is required to review the claims and correct all language which does not comply with 35 U.S.C. § 112, second paragraph.

***Claim Rejections - 35 USC § 102***

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless -
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

5. Claims 1, 2, 16, 20, 28, 29, 38, and 39 are rejected under 35 U.S.C. 102(e) as being anticipated by Agarwal (U.S. Patent No. 5,966,541), hereinafter referred to as Agarwal'541.

Referring to claim 1, Agarwal'541 discloses as claimed: a memory entry (the space containing blocks 101, 102 and 103 as shown in Fig. 8; Note a memory entry is best broadly and reasonable interpreted as a space where information can be stored and retrieved), storing a trace (including blocks 101, 102 and 103 as shown in Fig. 8) having a multiple-entry (from I2 to I3 and from I2 to I5, see Fig. 8), single exit (from I9 in block 103, see Fig. 8) architecture. Note Fig. 8 is best reasonably and broadly interpreted as to comprise many traces such as from block 101 to block 103 and from block 102 to block 103 as shown in Fig. 8. Note claim 38 recites the corresponding limitations as set forth in the claim 1.

Referring to claim 16, Agarwal'541 discloses as claimed: A processing engine (certainly existing in Agarwal'541's system), comprising: a front end stage to store blocks (in memory 703, see Fig. 11, and Col. 11, line 36), including blocks 101, 102 and 103 as shown in Fig. 8) of instructions in a multiple-entry (from I2 to I3 and from I2 to I5, see Fig. 8), single exit (from I9 in block 103, see Fig. 8) architecture when considered according to program flow, and an execution unit (certainly existing in Agarwal's system) in communication with the front end stage.

Referring to claim 20, Agarwal'541 discloses as claimed: apparatus, comprising a memory entry to store (in memory 703, see Fig. 11, and Col. 11, line 36) a sequence of program instructions (from I3 to I9 see Fig. 8) as a trace (including blocks 101, 102 and 103 as shown in Fig. 8), the instructions defining a program flow that progresses (note Fig. 8 shows the program flow progresses instruction to instruction) from any instruction (instructions from I3 to I8 see Fig. 8) therein to a last instruction (last instruction I9 see Fig. 8) in the trace and in which the trace has multiple separate prefixes (block 101 and block 102 are the prefixes as shown in Fig. 8).

Referring to claim 28, Agarwal'541 discloses as claimed: a trace (including blocks 101, 102 and 103 as shown in Fig. 8), comprising a sequence of program instructions (from I3 to I9 see

Fig. 8) stored together (in memory 703, see Fig. 11, and col. 11, line 36) assembled in order according to program flow, the sequence having a multiple-entry (from I2 to I3 and from I2 to I5, see Fig. 8), single exit (from I9 in block 103, see Fig. 8) architecture. Note as set forth above, Fig. 8 is best reasonably and broadly interpreted as to comprise many traces such as from block 101 to block 103 and from block 102 to block 103 as shown in Fig. 8.

As to claims 2, 29 and 39, Agarwal'541 also discloses: the trace being a complex trace (including blocks 101, 102 and 103 as shown in Fig. 8) having multiple independent prefixes (block 101 and block 102 as shown in Fig. 8) and a common, shared suffix (block 103 is the as shown in Fig. 8).

***Allowable Subject Matters***

6. Claims 4-7, 9-15, and 23-27 are allowed.

7. Claims 17-19 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

8. Claims 3, 22, 30, and 40 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

9. Claims 41-43 would be allowable if rewritten or amended to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action.

10. The following is a statement of reasons for the indication of allowable subject matter: Agarwal, the closest references, do not teach or fairly suggest:

a front-end system comprising: the extended block cache system having a block predictor to store masks associated with the complex traces, the masks distinguishing the prefixes from each other (in claim 4);

at least specifically the step of determining whether the predicted address matches an address of a terminal instruction of a previously created extended block (in claim 9); and

means for indexing the trace by an address of a last instruction therein according to program flow (in claim 23, and 41-43). Further, the combination of the limitations with the limitations of the respective independent claims is not obvious.

***Response to Arguments***

11. Applicant's arguments filed 10/4/04 have been fully considered but they are not deemed to be persuasive.

Regarding the 35 U.S.C. §112, second paragraph problems, Applicant's response has not completely overcome these rejections.

Regarding the 101 rejection under 35 U.S.C. 101, Applicant's arguments are deemed to be persuasive. The rejection has been withdrawn.

**As to claim 1, Applicants argue that Agarwal's blocks do not have a multiple entry, single exit architecture, but rather, each block has a single entry, single exit architecture. See Agarwal, col. 11, lines 17-20. More importantly, Agarwal does not disclose whether and/or how these blocks are stored in a memory entry, but simply that "some memory is associated with each program block". See Agarwal, col. 11, lines 36-38. Thus, Agarwal fails to disclose a memory entry storing a trace having a multiple-entry, single exit architecture (page 11, lines 3-8).**

Examiner disagrees with Applicants. In claim 1, **blocks** having a multiple entry, single exit architecture is not the claimed limitations. Instead, **a trace** having a multiple-entry, single exit architecture is the claimed limitation in claim 1.

As set forth above, Agarwal'541 discloses as claimed: a memory entry (the space containing blocks 101, 102 and 103 as shown in Fig. 8; Note a memory entry is best broadly and reasonable interpreted as a space where information can be stored and retrieved), storing **a trace** (including blocks 101, 102 and 103 as shown in Fig. 8) having a multiple-entry (from I2 to I3 and from I2 to I5, see Fig. 8), single exit (from I9 in block 103, see Fig. 8) architecture. Note Fig. 8 is best reasonably and broadly interpreted as to comprise many traces such as from block 101 to block 103 and from block 102 to block 103 as shown in Fig. 8. Note claim 38 recites the corresponding limitations as set forth in the claim 1. Regarding whether and/or how these blocks are stored in a memory entry, Agarwal'541 does disclose portions of this program flow are stored in a common memory entry in memory 703, see Fig. 11, and Col. 11, line 36. The common memory entry includes blocks 101, 102 and 103 as shown in Fig. 8 and multiple entries, from I2 to I3 and from I2 to I5, are also shown in Fig. 8.

As to claim 16, Applicants argue that "Again, Agarwal's **blocks do not have a multiple entry, single exit architecture, but rather, each block has a single entry, single exit architecture. See Agarwal, col. 11, lines 17-20. More importantly, Agarwal fails to disclose whether and/or how these**

**blocks are stored in a front-end stage having a multiple-entry, single exit architecture. Accordingly, Agarwal fails to anticipate the claimed invention as recited in claim 16" (page 11, lines 16-21).**

Examiner disagrees with Applicants. As set forth above, Agarwal'541 discloses **as claimed**: a front end stage to store blocks (in memory 703, see Fig. 11, and Col. 11, line 36), including blocks 101, 102 and 103 as shown in Fig. 8) of instructions in a multiple-entry (from I2 to I3 and from I2 to I5, see Fig. 8), single exit (from I9 in block 103, see Fig. 8) architecture when considered according to program flow, and an execution unit (certainly existing in Agarwal's system) in communication with the front end stage. Regarding whether and/or how these blocks are stored in a memory entry, again Agarwal'541 does disclose portions of this program flow are stored in a common memory entry in memory 703, see Fig. 11, and Col. 11, line 36. The common memory entry includes blocks 101, 102 and 103 as shown in Fig. 8 and multiple entries, from I2 to I3 and from I2 to I5, are also shown in Fig. 8.

As to claim 20, Applicants argue that "As explained above, **Agarwal's blocks do not have a multiple entry, single exit architecture, but rather, each block has a single entry, single exit architecture. Moreover, the program flow is defined by**

**putting together multiple instruction blocks in a sequential order. Thus, Agarwal's program flow cannot progress from any instruction to a last instruction in the memory entry. Rather, Agarwal's program flow must start with instruction IO of the first block and end with instruction 19 of the last block" (page 11, lines 29-32, and page 12, lines 1-2).**

Examiner disagrees with Applicants. As set forth above, Agarwal'541 discloses **as claimed**: a memory entry to store (in memory 703, see Fig. 11, and Col. 11, line 36) a sequence of program instructions (from I3 to I9 see Fig. 8) as a trace (including blocks 101, 102 and 103 as shown in Fig. 8), the instructions defining a program flow that progresses (note Fig. 8 shows the program flow progresses instruction to instruction) from any instruction (instructions from I3 to I8 see Fig. 8) therein to a last instruction (last instruction I9 see Fig. 8) in the trace and in which the trace has multiple separate prefixes (block 101 and block 102 are the prefixes as shown in Fig. 8). Further, Agarwal's program flow starting with instruction IO of the first block and ending with instruction 19 of the last block are not used to interpret the claim language. As set forth in the art rejections to claim 20, a sequence of program instructions, **from I3 to I9** see Fig. 8, is best reasonably and broadly interpreted as the claimed invention.

**As to claim 28, Applicants argue that "Aqarwal does not disclose a trace, or any equivalent structure thereof. Additionally, Agarwal's blocks do not have a multiple entry, single exit architecture, but rather, each block has a single entry, single exit architecture. See Aqarwal, col. 11, lines 17-20. More importantly, Agarwal does not disclose whether and/or how these blocks are stored in a trace. Thus, Agarwal fails to disclose a trace comprising an program instruction sequence having a multiple-entry, single exit architecture" (page 12, lines 12-17).**

Examiner disagrees with Applicants. Again, in claim 28, **blocks** having a multiple entry, single exit architecture is not the claimed limitations. Instead, **a trace** having a multiple-entry, single exit architecture is the claimed limitation in claim 1. As set forth above, Agarwal'541 discloses as claimed: a trace (including blocks 101, 102 and 103 as shown in Fig. 8), comprising a sequence of program instructions (from I3 to I9 see Fig. 8) stored together (in memory 703, see Fig. 11, and col. 11, line 36) assembled in order according to program flow, the sequence having a multiple-entry (from I2 to I3 and from I2 to I5, see Fig. 8), single exit (from I9 in block 103, see Fig. 8) architecture. Note as set forth above, Fig. 8 is best reasonably and broadly interpreted as to

comprise many traces such as from block 101 to block 103 and from block 102 to block 103 as shown in Fig. 8. Regarding whether and/or how these blocks are stored in a trace, Agarwal'541 does disclose portions of this program flow are stored in a common memory entry in memory 703, see Fig. 11, and Col. 11, line 36. The common memory entry includes a trace (including blocks 101, 102 and 103 as shown in Fig. 8); and the sequence of program instructions (from I3 to I9 see Fig. 8) having a multiple-entry (from I2 to I3 and from I2 to I5, see Fig. 8), single exit (from I9 in block 103, see Fig. 8) architecture.

In summary, Agarwal teaches the claimed invention.

***Conclusion***

12. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any

extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

***Contact Information***

**13.** Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dr. Henry Tsai whose telephone number is (571) 272-4176. The examiner can normally be reached on Monday-Thursday from 8:00 AM to 5:00 PM. If attempts to reach the examiner by telephone are unsuccessful, the examiner supervisor, Eddie Chan, can be reached on (571) 272-4162. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to **the TC central telephone number, 571-272-2100.**

14. In order to reduce pendency and avoid potential delays, Group 2100 is encouraging FAXing of responses to Office actions directly into **the Group at fax number: 703-872-9306.** This practice may be used for filing papers not requiring a fee. It may also be used for filing papers which require a fee by

applicants who authorize charges to a PTO deposit account. Please identify the examiner and art unit at the top of your cover sheet. Papers submitted via FAX into Group 2100 will be promptly forward to the examiner.

HENRY W. H. TSAI
PRIMARY EXAMINER

December 27, 2004